

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE CITATION

JUN 28 2004

(Use several sheets if necessary)

ATTY. DOCKET NO.
114596-26-0051BSSERIAL NO.
09/666,110

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APPLICANT

Korbin S. VAN DYKE, et al.

JUN 02 2004

FILING DATE

September 20, 2000

GROUP ART UNIT

2183

Technology 2100

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	4,636,940	01/1987	Goodwin	717	128	Dec. 20, 1985
	4,750,112	06/07/1988	Jones	364	200	Feb. 10, 1984
	5,168,557	12/01/1992	Shibuya	712	207	Sep. 21, 1989
	5,241,638	08/31/1993	Mork	711	207	Aug. 12, 1995
	5,339,422	8/16/1994	Brender	714	4	Mar. 7, 1991
	5,355,487		Keller			
	5,386,563	01/31/1995	Thomas	712	228	Oct. 13, 1992
	5,404,476	04/04/1995	Kadaira	711	207	Mar. 9, 1993
	5,483,647	01/09/1996	Yu	713	100	Dec. 17, 1992
	5,487,156	01/23/1996	Popsescu	712	217	Dec. 5, 1990
	5,507,028	04/09/1996	Liu	395	375	Jan. 9, 1995
	5,560,013	09/24/1996	Scalzi	717	138	Dec. 6, 1994
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	5,742,780	04/21/1998	Caulk	395	382	Jan. 16, 1997
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	5,819,064	10/06/1998	Razdan	703	27	Nov. 8, 1995
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	5,911,073	06/08/1999	Mattson	395	701	Dec. 23, 1997
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	6,141,683	10/31/2000	Kraml	709	220	Jan. 30, 1998
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	6,202,205	03/13/2001	Saboff	717	9	Jul. 21, 1998
	6,205,545	03/20/2001	Shah	712	237	Apr. 30, 1998
	6,212,493	04/03/2001	Huggins	703	22	Dec. 1, 1998
	6,233,678	05/15/2001	Bala	712	240	Nov. 5, 1998
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	6,453,292	09/17/2002	Ramaswamy	704	235	Oct. 28, 1998
	6,470,442	10/22/2002	Arimilli	712	32	Jul. 30, 1999
	6,473,846	10/29/2002	Melchior	711	170	Jun. 16, 2000
	6,549,930	04/15/2003	Chrysos	709	104	Nov. 26, 1997
	6,557,094	04/29/2003	Pechanek	712	209	Sep. 28, 2001
	6,560,693	05/06/2003	Puzak	712	207	Dec. 10, 1999
	6,591,414	07/08/2003	Hibi	717	151	Oct. 3, 1997
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RLE		Ammons, Ball and Larus: Exploiting Hardware Performance Counters with Flow and Context Sensitive Profiling, Proceedings of the ACM SIGPLAN 1997 Conference on Programming Language Design and Implementation, pp. 85-96 (1997)
RLE		Dean, ProfileMe: Hardware Support for Instruction-Level Profiling on Out-of-Order Processors, IEEE 1997, pp. 292-302
RLE		Reiner W. Hartenstein, Jürgen Becker: Performance Analysis in CoDe-X Partitioning for Structural Programmable Accelerators; Proc. of 5th Int'l Workshop on Hardware/Software Co-Design CODES/CASHE '97, Braunschweig, Germany, p. 141 (March 1997)
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RLE		Intel Corporation, Intel Processor Family Developer's Manual (1997), pages 1-1 to 1-6, 2-1 to 2-20
RLE		Intel Corporation, Intel Processor Family Developer's Manual (1997), vol. 3 (Architecture and Programming Manual), pages 3-1 to 3-3, 3-10 to 3-13, 12-1 to 12-27, 14-1 to 14-30
RLE		Jones, Puzzling with Microcode, ACM SIGARCH Computer Architecture News, vol. 11, no. 5, pp. 8-12 (1983)
		Kim and Tyson: Analyzing the Working Set Characteristics of Branch Execution, Proceedings of the 31st Annual ACM/IEEE International Symposium on Microarchitecture, pp. 49-58 (Dec. 1998)

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Sheet 4 of 4

FORM PCT/1449
PATENT & TRADEMARK OFFICEU.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

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ATTY. DOCKET NO.
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APPLICANT

Korbin S. VAN DYKE, et al.

FILING DATE
September 20, 2000 GROUP ART UNIT
2183OTHER DOCUMENTS (*Including Author, Title, Date, Pertinent Papers, Etc.:*)

RCE	M. Lipasti and J. Shen. Exceeding the Data-Flow Limit Via Value Prediction, 29th International Symposium on Microarchitecture, pages 226-237, IEEE (Dec. 1996)
RLE	Magnusson and Werner, Efficient Memory Simulation in SimICS, Proceedings of the 28th Annual Simulation Symposium, IEEE, pp. 62-73 (1995).
RLE	Mueller, Rustagi and Baker: MiThOS - A Real-Time Micro-Kernel Threads Operating System, IEEE Real-Time Systems Symposium 1995: pp. 49-55 (1995)
RLE	Park et al., Evaluation of Scheduling Techniques on a SPARC-Based VLIW Testbed, Proceedings of the 30th annual ACM/IEEE international symposium on Microarchitecture, pp. 104-113 (1997)
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EXAMINER

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Sheet 5 of 5

FORM PTO-1449 O INFORMATION DISCLOSURE CITATION DEU 02/04/2003	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE (Use several sheets if necessary)	ATTY DOCKET NO. 114596/05-4013	SERIAL NO 09/239,194
	APPLICANT John S. Yates, Jr., et al.	FILING DATE January 28, 1999	GROUP ART UNIT 2127

FOREIGN PATENT DOCUMENTS

KT	DOCUMENT NUMBER WO 98/28689 Wing	DATE 07/02/1998	COUNTRY PCT/US	CLASS G06F	SUBCLASS 11/00	TRANSLATION YES NO
KT	WO 98/38575 Klaiber	09/03/1998	PCT/US	G06F	11/00	RECEIVED
KT	WO 99/08188 Kelly	02/18/1999	PCT/US	G06F	11/00	DEU 04 2003
KT	WO 99/08191 Kelly	02/18/1999	PCT/US	G06F	12/00	Technology Center 2100

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KT	T.M. Conte, et al., "Accurate and practical profile-driven compilation using the profile buffer," Proceedings of the 29 th Annual International Symposium on Microarchitecture, Paris, France, pp. 36-45 (Dec. 1996)
KT	T.M. Conte, et al., "Hardware based profiling: An effective technique for profile-driven optimization," International Journal of Parallel Programming, vol. 24, no. 2 (Feb. 1996)
KT	T.M. Conte, et al., "Using branch handling hardware to support profile-driven optimization," Proceedings of the 27 th Annual International Symposium on Microarchitecture San Jose, CA (Dec. 1994)
KT	J.S. Cox et al., "Commercializing profile-driven optimization." Proceedings of the 28 th Hawaii International Conference on System Sciences, vol. 1 Maui, HI, pp. 221-228 (Jan. 1995)
KT	Dean, ProfileMe: Hardware Support for Instruction-Level Profiling on Out-of-Order Processors, IEEE 1997, pp. 292-302
KT	R.E. Hank, et al., Proceeding of the 28 th Annual International Symposium on Microarchitecture, pp. 158-168 (Dec. 1995)
KT	Kavi et al., A Performability Model for SoR Real-Time Systems, IEEE Jan 1994
KT	Kim and Tyson: Analyzing the Working Set Characteristics of Branch Execution, IEEE 1998
KT	Larus and Schnarr: EEL/Machine-Independent Executable Editing, ACM Sigplan, 1995
KT	Lipasti and Shen: Exceeding the Dataflow Limit via Value Prediction, IEEE, 1996
KT	K.N.P. Menezes, "Hardware-based profiling for program optimization," Ph.D. thesis, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina (1997)
KT	Veen: Dataflow Machine Architecture, ACM Computing Surveys vol. 18 no. 4 pp. 365-96 (December 1986)
EXAMINER <i>Kenneth Ig</i>	DATE CONSIDERED 6/12/04

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PATENT

ATTORNEY DOCKET NO. 114596-26-0051BS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.: 09/666,110 Confirmation No.: 1446
Applicant: Korbin S. Van Dyke, et al.
Title: COMPUTER FOR EXECUTION OF RISC AND CISC INSTRUCTION
SETS
Filed: September 20, 2000
Art Unit: 2183
Examiner: R. Ellis
Atty. Docket: 114596-26-0051BS
Customer No. 38492

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In accordance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant wishes to make of record the enclosed items, as listed on the accompanying Form PTO-1449. Applicant respectfully requests the Examiner to fully consider the items and independently ascertain their teaching before issuance of the next action, and to make them of record in the file. The Examiner is also requested to initial and return a copy of the enclosed Form PTO-1449 to evidence such consideration.

1. Applicant has listed publication dates on the attached Form PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated. Applicant reserves the right to establish the patentability of the claims over any information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered. This Information Disclosure Statement should not be construed as a representation that information more material to the examination of this application does not exist.
2. The references listed on the enclosed Form 1449 are references that have come to light in applications listed in the Information Disclosure Statement of February 2001. Applicant has not reviewed

I certify that this correspondence, along with any documents referred to therein, is being transmitted by facsimile on November 8, 2004 to Mail Stop AF, Art Unit 2183 at FAX no. 703 872 9306 Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Application Serial No. 09/666,110
Atty. Docket No. 114596-26-0051BS

all of them in detail. Of those that have been reviewed, none of the references are believed to be any more pertinent than the references provided in earlier IDS' and Forms 1449. However, in an abundance of caution, Applicant requests that they be considered.

3. For non-patent items listed on the enclosed Form PTO-1449 for which a copy is not already made of record in this application, a copy was previously cited by or submitted to the Patent and Trademark Office in application Serial No. 09/239,194, filed January 28, 1999, Yates et al., Executing Programs for a First Computer Architecture on a Computer of a Second Architecture, in application Serial No. 09/322,443, filed May 28, 1999, Reese et al., Profiling of Computer Programs Executing in Virtual Memory Systems, or in application Serial No. 09/385,394, filed August 30, 1999, Yates et al., Computer for Executing Two Different Instruction Sets, or in application 09/626,325, filed July 26, 2000, Yates, et al., Computer with Two Operating Systems.

4. This Information Disclosure Statement it is being filed at a time when prosecution is closed, but may be reopened. In the event of reopening of prosecution, entry of this Information Disclosure Statement is proper on payment of a fee pursuant to 37 C.F.R. §1.97(c)(2). Upon such entry, charge the fee due under C.F.R. §1.17(i)(1) to 23-2405, Order No. 114596-26-0051BS.

5. Charge the fee due under C.F.R. §1.17(p) to Deposit Account 23-2405, Order No. 114596-26-0051BS. A DUPLICATE COPY OF THIS SHEET IS ATTACHED.

6. The Commissioner is hereby authorized to charge any additional fees that may be required for this Information Disclosure Statement, or credit any overpayment, to Deposit Account No. 23-2405, Order No. 114596-26-0051BS.

Respectfully submitted,

WILLKIE FARR & GALLAGHER LLP

Dated: November 8, 2004

By: David E. Boundy

David E. Boundy
Registration No. 36,461

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787 Seventh Ave.
New York, New York 10019
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Sheet 1 of 4

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			ATTY. DOCKET NO. J14596-26-0051BS	SERIAL NO. 09/666,110		
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	4,636,940	01/1987	Goodwin	717	.128	Dec. 20, 1985
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